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*Introduction to*

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*Precision Time*

*Protocol (PTP)*

**Synchronizing**

**Networks with**

**IEEE 1588 PTP**

**IEEE 1588 PTP**

**synchronization**

**- OSA 5420**

**Series Precision**

Time Protocol

(PTP) Clock

Types Lesson 22

- VHDL Example

10: Generic MUX

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Ptp Parameters.ppt

*Challenge: SyncE  
and IEEE-1588*

*Packet*

*Synchronization  
(Part 4/7)*

Precision Time

Protocol (IEEE

1588): main

features Testing

PTP Clocks in

the Lab SPAG:

*Clocking \u0026*

*Sync Part 1/3:*

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*TDM and Packet-  
based Frequency  
Sync Precision*

**Time Protocol**

**(PTP) and Packet**

**Timestamping in**

**Linux - Antoine**

**Tenart, Bootlin**

VHDL Lecture 1

VHDL Basics #15

Part 1: UART-TxD

Serial

Communication

using an FPGA

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Board | Verilog

? Step-by-Step

Instructions

*What is a UART*

*in an FPGA?*

*Basics of Serial*

*Ports, COM Port,*

*RS-232, RS-485*

*Amplitude,*

*Frequency, and*

*Phase What is a*

*Block RAM in an*

*FPGA? What is*

*SPI? Basics for*



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Electronics

Interview

Questions: FIFO

Buffer Depth

Calculation

~~How to Begin a~~

~~Simple FPGA~~

~~Design How I2C~~

~~Communication~~

~~Works and How To~~

~~Use It with~~

~~Arduino 0TMC~~

~~100: Using NTP~~

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~~and PTP at the~~

~~same time What~~

~~is Precision~~

~~Timing? | Sync~~

~~102 Stanford~~

~~Seminar~~

~~Nanosecond level~~

~~Clock~~

~~Synchronization~~

~~in a Data Center~~

~~SPAG: Clocking~~

~~\u0026 Sync Part~~

~~2/3: IEEE 1588~~

~~and PTPv2 What~~

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*is I2C, Basics*

*for Beginners*

*What is a FIFO*

*in an FPGA*

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*Questions for a*

*job in FPGA,*

*VHDL, Verilog*

*How to read*

*button press in*

*VHDL* **Keeping**

**Time with PTP -**

**Michael Waidson,**

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**Tektronix** More

*Deterministic*

*Software for*

*Cyber-Physical*

*Systems* ~~DP83640~~

~~10/100 IEEE 1588~~

~~Time Sync Demo~~

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Hardware

Implementation

Vhdl

Many variants

for implementing

the Precision

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Time Protocol

(PTP) exist,  
such as software  
only

implementations  
or hardware  
assisted  
software  
implementations.

This work  
describes a  
hardware  
implementation  
of PTP which is

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fully coded in  
VHDL (Hardware  
assisted  
hardware  
implementation) .

IEEE1588 PTP

Hardware

Implementation

in VHDL:

IEEE1588 ...

This Application  
Note describes  
the overview

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Concept of IEEE  
1588v2 standard  
and Precision

Time Protocol as  
well as the  
procedure and  
architecture of  
Altera 1588  
system solution  
reference design  
using Altera  
Arria V SoC, 10G  
Ethernet MAC  
with 10G BASE-R

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PHY hardware IP  
and software  
stack which is  
build based on  
Linux kernel  
v3.16, consists  
of PTP stack  
LinuxPTP v1.5, a  
preloader, 10G-  
bps Ethernet MAC  
driver and a PTP  
driver.

Altera 1588

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System Solution

- Intel

White Paper Hard

ware-Assisted

IEEE 1588\*

Implementation

March 2005

Document Number:

305068,

Revision: 001 5

1.0 Introduction

This document

describes a hard

ware-assisted

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IEEE 1588\*  
implementation  
in the IXP46X  
product line of  
network

processors. An  
overview of the  
1588 standard is  
presented, and  
the general pros

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Implementation  
in the Intel...

The IEEE 1588

PTP can also be  
implemented

solely in

software, while

IEEE 1588

hardware time

stamping can be

performed by

connecting an

FPGA between the

Ethernet PHY and

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MAC. The FPGA  
time stamps each  
incoming and  
outgoing SYNC  
and  
DELAY\_REQUEST  
message.

Utilizing FPGAs  
in an IEEE 1588  
Precision Time  
Control ...

PreciseTimeBasic  
is a

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### IEEE1588-2008 V2

### compliant clock synchronization

### IP core for

### Xilinx FPGAs. It

### is capable of

### accurately time

### stamp IEEE 1588

### telegrams and

### also to provide

### a compatible

### time.

### PreciseTimeBasic

### IP comprises

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different hardware  
hardware and  
software  
elements - A  
hardware Time  
Stamping Unit  
(TSU) capable of  
accurately time  
stamp IEEE 1588  
event messages  
and to provide  
an adjustable  
timer ...

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implementation

of IEEE 1588

protocol for

IEEE 802.11

WLAN. ...

location

detection and

energy

conservation.

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Protocol (PTP)  
is a widely used  
clock  
synchronization  
...

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implementation  
of IEEE 1588  
protocol for  
IEEE 802 ...

IEEE1588 PTP  
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Hardware  
Implementation  
Vhdl  
Assisted IEEE  
1588 IP Core.

The necessary  
FPGA logic to  
assist SW  
protocol stack  
in implementing  
the Precision  
Time Protocol  
(IEEE 1588-2008)  
on

1000M/100M/10M

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Ethernet

networks. PTP  
packets

transmitting and  
receiving should  
be implemented  
by PTP SW  
protocol stack  
(PTPd) with  
existing MAC  
function; This  
IP Core  
implements the  
Real-Time ...

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Assisted IEEE

1588 IP Core ::

OpenCores

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Protocol daemon

for free.

Portable,

complete and BSD-

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1588 (PTP)

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Implementation.

The PTP daemon  
(PTPd)

implements the  
Precision Time  
protocol (PTP)  
as defined by  
the IEEE 1588  
standard. PTP  
was developed to  
provide very  
precise time  
coordination of  
LAN connected

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Implementation

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PTP development

overview - Mixt

software /

hardware PTP

implementation

PTPd Software

(Kendall &

Corell) Without

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linux network

API HARDWARE :

NIOS cpu

softcore in VHDL

(targetted in

FPGA) Gigabit

MAC IP (from

I.F.I. German

society) PTP Cl

k i l i i VHD

DDR sdram FPGA

ALTERA STRATIX

II PTP Clock

implemtation in

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VHDL Time stamp  
unit PTP frame  
detector

PTP version 1  
implementation  
on FPGA ith NIOS  
dFPGA with ...

The PTP  
Grandmaster  
Clock (GM) from  
NetTimeLogic is  
a full hardware  
only



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Implementation

of a GM as  
defined in

IEEE1588-2008.

It implements  
all algorithms  
directly in  
hardware, no  
software or soft-  
core CPU is  
needed. The  
Grandmaster  
Clock is based  
on the OC and

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allows  
additional  
synchronization  
of the clock  
which shall be  
distributed.

NetTimeLogic

GmbH - PTP

Products

In a simple  
IEEE-1588 PTP  
implementation,  
a few PTP-

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Enabled Ethernet devices connect to a switch with one device acting as master clock. The devices synchronize with the primary clock, establishing a common time within the network.

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Hardware  
Implementation  
in VHDL : Gerald

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syn1588 PTP  
Stack from  
Oregon Systems:  
A portable  
implementation  
of the complete

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IEEE1588-2008

standard with  
special features

like Boundary

Clock support,

Unicast

operation, IPv6

support and

security

enhancements.

List of PTP

implementations

- Wikipedia

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The syn1588 ©

PTP Stack's  
software

architecture is  
partitioned into  
the PTP library  
and the PTP  
application. The  
library executes  
a protocol  
engine which  
processes PTP  
messages and  
drives a control

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loop to  
synchronize a  
(hardware)  
clock. The  
engine is  
designed as a  
state machine  
according to the  
full  
master/slave  
state protocol  
of the  
IEEE1588-2008  
standard.



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NetTimeLogic's  
PTP Ordinary  
Clock is a full  
hardware (FPGA)  
only  
implementation  
of an Ordinary  
Clock according  
to IEEE1588-2008  
(PTP). The whole

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protocol  
handling,  
algorithms and  
calculations are  
implemented in  
the core, no CPU  
is re-quired.  
This allows  
running PTP  
synchronization  
completely  
independent and  
standalone from  
the user

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Application.  
Implementation  
PtpOrdinaryClock  
- Nettimelogic  
GmbH

PreciseTime  
Basic is a  
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compliant clock  
synchronization  
IP core for  
Xilinx FPGAs. It  
is capable of  
accurately time

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stamp IEEE 1588  
telegrams and  
also to provide  
a compatible  
timer. All these  
processes are  
carried out by  
hardware  
modules.

PreciseTimeBasic  
: IEEE 1588-2008  
IP Core

The PTP Ordinary

*Page 44/48*

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Clock (OC) from  
NetTimeLogic is  
a combination of  
NetTimeLogic's  
PTP Transparent  
Clock (TC) and  
PTP Ordinary  
Clock (OC). It  
adds the Sync  
and Announce  
message  
processors to  
the design which  
allow

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Synchronization  
of the clock  
according to  
IEEE1588 while  
keeping the  
timing aware  
frame forwarding  
feature of the  
TC.

PTP Hybrid Clock  
- xilinx.com

It also shows  
that although

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the Cisco Nexus  
3548 has  
nanosecond PTP  
accuracy, the  
server is  
causing a lot of  
offset with a  
pure software  
PTP  
implementation.  
Hardware PTP on  
the server is  
required for  
better PTP

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accuracy.

Hardware PTP: 44

Servers. The

hardware PTP

test uses 44

servers running

hardware PTP.

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